of charge in the collector at a voltage less than collector-emitter breakdown voltage.

FIGS. 2 and 3 illustrate the D.C. characteristics, plotting collector current versus collector-emitter voltage, for two similar integrated transistors. The BV_{CBO} of the devices are identical, that is, the collector-base breakdown voltages of these devices are identical. However, the device of FIG. 3 is provided with a buried layer whereby depletion in the collector region is not procured due to the charge carriers available from the buried layer. In the FIG. 2 device, no buried layer is present, and the thickness and doping of the collector are such that virtually complete charge depletion in the collector takes place. Breakdown is indicated at the right hand extremities of the curves in each instance, which are plotted for various values of base current). It is seen that breakdown occurs in the buried layer device illustrated in FIG. 3 much before the device for which the characteristics are plotted in FIG. 2. The BV_{CEO} of the device, the characteristics of which are plotted in FIG. 3, is less than half of the BV_{CEO} of the device the characteristics of which are portrayed in FIG. 2.

Another significant difference is also evident in that the output impedance of the device of FIG. 2 is much greater as indicated by the flatter curves. This is the result of limiting the collector-base space charge layer width in the active base, thus eliminating collector current variations due to base-width modulation. That is, the top of the space charge layer **42** is fixed, and does not move up and down with changes in collector-emitter voltage.

The curves for FIG. 4 were taken from the same device as were the curves in FIG. 2. However, a much higher substrate bias is applied in the instance of the device operated in the manner illustrated in FIG. 4. Since the maximum current in the device is determined by the relatively low carrier density in the constricted collector region, the collector current attains a substantially maximum value regardless of changes in base current.

It should be understood that an NPN transistor device is illustrated by way of example, and that the invention is also applicable to PNP devices.

While I have shown and described preferred embodiments of my invention, it will be apparent to those skilled in the art that many changes and modifications may be made without departing from my invention in its broader aspects. I therefore intend the appended claims to cover all such changes and modifications as fall within the true spirit and scope of my invention.

I claim:

1. A transistor device comprising:

an integrated circuit substrate of first conductivity type material and a collector providing layer of a second conductivity type material disposed on a single side of the substrate with one side of said layer forming a PN junction with the substrate, said layer, having the other side, disposed opposite the substrate, containing a base region of first conductivity type material and an emitter region of second conductivity type material within the base region with surfaces exposed at said other side of the layer,

said layer having means for depletion of virtually all majority carriers from the active collector region thereof between said base region and substrate upon application of a collector-emitter voltage less than the collector-emitter breakdown voltage value for the device with the base open circuited.

2. The transistor device according to claim **1** wherein restriction of the thickness and resistivity of the active collector region produces said depletion upon application of a voltage below the collector-emitter breakdown voltage for the device.

3. The transistor device according to claim **1** wherein said active collector region has a thickness, t, measured in centimeters less than

$$\sqrt{\frac{2\epsilon V}{qN}}$$

wherein ϵ is the dielectric constant of the collector semiconductor material, q is the charge of an electron, N is the substantially constant impurity densiy of the collector semiconductor material, and V is the voltage for collector-emitter breakdown of said device without restriction in thickness of said collector region, whereby the active collector region is substantially depleted of majority carriers upon application of a voltage below the value for collector-emitter breakdown of the device.

4. The transistor device according to claim **3** wherein said PN junction with said substrate is back-biased to provide a second depletion region in the collector the edge of which defines one boundary of the active collector region, t being measured from such boundary to the collector-base junction.

5. The transistor device according to claim **3** wherein the base region is more heavily doped than the collector region.

6. The transistor device according to claim **3** wherein said layer comprises semiconductor material epitaxially grown on the substrate and appropriately doped to provide said regions.

7. The transistor device according to claim **3** in which such substantial depletion takes place in the collector region before the collector-base space charge layer in the base region extends to the emitter region.

References Cited

UNITED STATES PATENTS

3,404,295 10/1968 Warner ---------- 307—302

JAMES D. KALLAM, Primary Examiner

U.S. Cl. X.R.

317—234